What is claimed is:

1. A display driver which drives a plurality of data lines of an electro-optical device that includes a plurality of pixels, a plurality of scan lines, and the data lines, the display driver comprising:

an instruction signal generation circuit which generates a data-fetch-start-instruction-signal;

a data latch which fetches display data at data fetch timings including a fetch start timing that is determined by the data-fetch-start-instruction-signal; and

a data line drive circuit which drives the data lines, based on the display data fetched into the data latch,

wherein the instruction signal generation circuit includes a fetch-start-timing-setting-register into which is set data for determining the fetch start timing of the display data, and

wherein the instruction signal generation circuit generates the data-fetch-start-instruction-signal that changes when a period corresponding to the data set in the fetch-start-timing-setting-register has elapsed, with reference to a reference timing.

2. The display driver as defined in claim 1,

wherein the data for determining the fetch start timing is data corresponding to a period up until the fetch start timing of the display data, with reference to a transition point in a horizontal synchronization signal that determines one horizontal scan period, and

wherein the reference timing is the transition point in the horizontal synchronization signal.

3. The display driver as defined in claim 2,

wherein the data corresponding to the period up until the fetch start timing of the display data is a number of clocks of a reference clock up until the fetch start timing of the display data, with reference to the transition point in the horizontal synchronization signal, and

wherein the display data is supplied to the data latch in synchronization with the reference clock.

4. The display driver as defined in claim 3,

wherein the instruction signal generation circuit comprises:

a counter having a count value which is reset based on the horizontal synchronization signal and incremented at a transition point of the reference clock;

a comparator which compares the count value and the data set in the fetch-start-timing-setting-register; and

a flip-flop which holds a comparison result signal of the comparator at the transition point of the reference clock,

wherein the data-fetch-start-instruction-signal is a signal that is held in the flip-flop of the instruction signal generation circuit and output to the data latch.

5. The display driver as defined in claim 1,

wherein the data latch comprises:

a shift register having a plurality of flip-flops, which shifts the data-fetch-start-instruction-signal based on the reference clock, and outputs a shift output from each of the flip-flops; and

a latch having a plurality of flip-flops, each of which holds the display data based on the shift output.

6. The display driver as defined in claim 2,

wherein the data latch comprises:

a shift register having a plurality of flip-flops, which shifts the data-fetch-start-instruction-signal based on the reference clock, and outputs a shift output from each of the flip-flops; and

a latch having a plurality of flip-flops, each of which holds the display data based on the shift output.

7. The display driver as defined in claim 3,

wherein the data latch comprises:

a shift register having a plurality of flip-flops, which shifts the data-fetch-start-instruction-signal based on the reference clock, and outputs a shift output from each of the flip-flops; and

a latch having a plurality of flip-flops, each of which holds the display data based on the shift output.

8. The display driver as defined in claim 4,

wherein the data latch comprises:

a shift register having a plurality of flip-flops, which shifts the data-fetch-start-instruction-signal based on the reference clock, and outputs a shift output from each of the flip-flops; and

a latch having a plurality of flip-flops, each of which holds the display data based on the shift output.

9. The display driver as defined in claim 1, further comprising:

a mode setting register for setting the display driver into a master mode that is a mode in which the data-fetch-start-instruction-signal is generated by the instruction

signal generation circuit or a slave mode that is a mode in which an enable input signal is received from the outside of the display driver; and

a switching circuit which outputs the data-fetch-start-instruction-signal or the enable input signal to the data latch, in accordance with the mode set by the mode setting register,

wherein the switching circuit selects and outputs the data-fetch-start-instruction-signal when the display driver is set to the master mode by the mode setting register, and selects and outputs the enable input signal when the display driver is set to the slave mode by the mode setting register; and

wherein the data latch fetches the display data, based on the output from the switching circuit.

10. The display driver as defined in claim 2, further comprising:

a mode setting register for setting the display driver into a master mode that is a mode in which the data-fetch-start-instruction-signal is generated by the instruction signal generation circuit or a slave mode that is a mode in which an enable input signal is received from the outside of the display driver; and

a switching circuit which outputs the data-fetch-start-instruction-signal or the enable input signal to the data latch, in accordance with the mode set in the mode setting register,

wherein the switching circuit selects and outputs the data-fetch-start-instruction-signal when the display driver is set to the master mode by the mode setting register, and selects and outputs the enable input signal when the display driver is set to the slave mode by the mode setting register; and

wherein the data latch fetches the display data, based on the output from the switching circuit.

11. The display driver as defined in claim 3, further comprising:

a mode setting register for setting the display driver into a master mode that is a mode in which the data-fetch-start-instruction-signal is generated by the instruction signal generation circuit or a slave mode that is a mode in which an enable input signal is received from the outside of the display driver; and

a switching circuit which outputs the data-fetch-start-instruction-signal or the enable input signal to the data latch, in accordance with the mode set in the mode setting register,

wherein the switching circuit selects and outputs the data-fetch-start-instruction-signal when the display driver is set to the master mode by the mode setting register, and selects and outputs the enable input signal when the display driver is set to the slave mode by the mode setting register; and

wherein the data latch fetches the display data, based on the output from the switching circuit.

12. The display driver as defined in claim 4, further comprising:

a mode setting register for setting the display driver into a master mode that is a mode in which the data-fetch-start-instruction-signal is generated by the instruction signal generation circuit or a slave mode that is a mode in which an enable input signal is received from the outside of the display driver; and

a switching circuit which outputs the data-fetch-start-instruction-signal or the enable input signal to the data latch, in accordance with the mode set in the mode setting register,

wherein the switching circuit selects and outputs the data-fetch-start-instruction-signal when the display driver is set to the master mode by the mode setting register, and selects and outputs the enable input signal when the display driver is set to the slave mode by the mode setting register; and

wherein the data latch fetches the display data, based on the output from the switching circuit.

13. The display driver as defined in claim 5, further comprising:

a mode setting register for setting the display driver into a master mode that is a mode in which the data-fetch-start-instruction-signal is generated by the instruction signal generation circuit or a slave mode that is a mode in which an enable input signal is received from the outside of the display driver; and

a switching circuit which outputs the data-fetch-start-instruction-signal or the enable input signal to the data latch, in accordance with the mode set in the mode setting register,

wherein the switching circuit selects and outputs the data-fetch-start-instruction-signal when the display driver is set to the master mode by the mode setting register, and selects and outputs the enable input signal when the display driver is set to the slave mode by the mode setting register; and

wherein the data latch fetches the display data, based on the output from the switching circuit.

14. An electro-optical device comprising:

a plurality of pixels;

a plurality of scan lines;

a plurality of data lines; and

the display driver as defined in claim 1, which drives the data lines.

15. An electro-optical device comprising:

a display panel including a plurality of pixels, a plurality of scan lines, and a plurality of data lines; and

the display driver as defined in claim 1, which drives the data lines.

16. An electro-optical device comprising:

a plurality of pixels;

a plurality of scan lines;

a plurality of data lines; and

at least two of the display drivers as defined in claim 9, which drives the data lines,

wherein one of the at least two display drivers is set to the master mode,

wherein the remainder of the at least two display drivers is set to the slave mode, and

wherein the display driver that is set to the master mode supplies the enable input signal to at least one of the display drivers that has been set to the slave mode.

17. An electro-optical device comprising:

a plurality of pixels;

a plurality of scan lines;

a plurality of data lines; and

at least two of the display drivers as defined in claim 10, which drives the data lines,

wherein one of the at least two display drivers is set to the master mode,

wherein the remainder of the at least two display drivers is set to the slave mode, and

wherein the display driver that is set to the master mode supplies the enable input signal to at least one of the display drivers that has been set to the slave mode.

18. An electro-optical device comprising:

a plurality of pixels;

a plurality of scan lines;

a plurality of data lines; and

at least two of the display drivers as defined in claim 11, which drives the data lines,

wherein one of the at least two display drivers is set to the master mode,

wherein the remainder of the at least two display drivers is set to the slave mode, and

wherein the display driver that is set to the master mode supplies the enable input signal to at least one of the display drivers that has been set to the slave mode.

19. An electro-optical device comprising:

a plurality of pixels;

a plurality of scan lines;

a plurality of data lines; and

at least two of the display drivers as defined in claim 12, which drives the data lines,

wherein one of the at least two display drivers is set to the master mode,

wherein the remainder of the at least two display drivers is set to the slave mode, and

wherein the display driver that is set to the master mode supplies the enable input signal to at least one of the display drivers that has been set to the slave mode.

20. An electro-optical device comprising:

a plurality of pixels;

a plurality of scan lines;

a plurality of data lines; and

at least two of the display drivers as defined in claim 13, which drives the data lines,

wherein one of the at least two display drivers is set to the master mode,

wherein the remainder of the at least two display drivers is set to the slave mode, and

wherein the display driver that is set to the master mode supplies the enable input signal to at least one of the display drivers that has been set to the slave mode.

21. An electro-optical device comprising:

a display panel including a plurality of pixels, a plurality of scan lines, and a plurality of data lines; and

at least two of the display drivers as defined in claim 9, which drives the plurality of data lines,

wherein one of the at least two display drivers is set to the master mode,

wherein the remainder of the at least two display drivers is set to the slave mode, and

wherein the display driver that is set to the master mode supplies the enable input signal to at least one of the display drivers that has been set to the slave mode.